In the Claims:

Please amend claim 1 as indicated below. This listing of claims replaces all prior versions.

1. (currently amended) A bus system comprising a first and second station coupled via a bus for transferring data and control signals, the bus operating according to a protocol in which the first station repeatedly sends requests for data to the second station, the second station responding to each request by sending a message with a data item or sending a negative acknowledge signal, wherein the second station comprises:

an interruptable processor for generating data items;

a first in first out buffer coupled between the processor and the bus, for buffering data items for successive messages in a first in first out order, the processor being programmed to start writing the data items to the buffer in response to an interrupt;

a bus interface arranged to handle the protocol, sending data items from the buffer in the messages, the bus interface determining to send ~~sending~~ an interrupt to the processor in response to selected ones of the requests, as a function of whether ~~when~~ the buffer is empty and [[no]] whether interrupts have yet been generated since the processor has written into the buffer.

2. (original) A bus system according to Claim 1, wherein the bus system is a USB bus system.

3. (previously presented) A bus system according to claim 1, wherein the bus interface is arranged generate an interrupt signal in response to an acknowledge signal from the first station after sending the message.

4. (previously presented) A bus interface integrated circuit, comprising:

a connection for a bus;

a first in first out buffer;

an interrupt output for applying an interrupt to a processor;

a controller arranged to receive requests for data from the connection, and to respond to the requests by sending a message containing a data item from the buffer if the buffer is not empty, or by sending a negative acknowledge signal to the connection if the

buffer is empty and to send an interrupt signal to the interrupt output when the buffer is empty on receiving one of the requests, but only if no interrupt has yet been sent since data has been written into the buffer.

5. (previously presented) An integrated circuit according to claim 4, arranged to generate an interrupt signal in response to an acknowledge signal from the bus after sending the message.

6. (previously presented) An integrated circuit according to claim 4, arranged to be switchable between a plurality of modes of operation, the integrated circuit generating the interrupt signal to the interrupt output when the buffer is empty on receiving one of the requests, but only if no interrupt has yet been sent since data has been written into the buffer in a first one of the modes, the integrated circuit generating an interrupt signal in response to an acknowledge signal from the bus after sending the message in a second one of the modes.

7. (previously presented) An integrated circuit according to claim 4, arranged to be switchable between a plurality of modes of operation, the integrated circuit generating said interrupt signal in response to each request for data when the buffer is empty in a first one of the modes, the integrated circuit generating the interrupt signal to the interrupt output when the buffer is empty on receiving one of the requests, but only if no interrupt has yet been sent since data has been written into the buffer in a second one of the modes.

8. (previously presented) A station for connection to a bus, the station comprising:

a connection for a bus;

a processor;

a first in first out buffer;

an interrupt output coupled to the processor;

a controller arranged to receive requests for data from the connection, and to respond to the requests by sending a message containing a data item from the buffer if the buffer is not empty, or by sending a negative acknowledge signal to the connection if the buffer is empty and to send an interrupt signal to the interrupt output when the buffer is

empty on receiving one of the requests, but only if no interrupt has yet been sent since data has been written into the buffer.

9. (original) A station for connection to a bus according to Claim 8, arranged to operate as a USB station.